When it comes to double-density Flash memory, some pairs are just better.

AMD pairs high-performance with reliability in a single Flash memory cell, with revolutionary results.

**Introducing MirrorBit™**

Flash Memory without Compromise

MirrorBit technology is a breakthrough memory cell architecture that – for the first time – enables a Flash memory product to hold twice as much data without compromising performance or data integrity. Specially engineered by AMD, MirrorBit technology presents a better way to store a pair of bits in one cell. Which means better performance, better reliability, and better cost for AMD customers – without compromise.

**MirrorBit Overview**

**What Is MirrorBit™?**

MirrorBit technology is an industry first – the first to store two bits of data in one memory cell – and double device density – without compromising data integrity or system performance. AMD created the MirrorBit architecture using a radical new design and process technology. This new architecture offers customers a low-cost, highly reliable Flash memory solution.

**How Does It Work?**

The MirrorBit architecture stores two bits of data in distinct charge areas within a single cell. By storing electrons in two physically different locations, MirrorBit technology delivers two bits, or “transistors,” which can be read or programmed independently at full power.

Compared to conventional Flash, MirrorBit Flash offers:

- Double the storage capacity
- Equally high performance and reliability
- A better cost structure

**Key Benefits**

Other key benefits include:

- Ease of use, with the same packages and pin-outs as our current LV family of products
- An easy migration path all the way to 1 gigabit
- AMD’s award-winning service and support

**MirrorBit™ Brings New Features to Flash Memory Devices**

MirrorBit Flash offers speed-enhancing page buffers to further improve functionality and device performance. By increasing read performance by 3 to 4 times and write performance by up to 16 times, these buffers significantly improve how fast data moves in and out, and so reduce the bottleneck inherent to high-density Flash devices.

**What About Cost?**

MirrorBit technology offers the best cost structure in the industry. Its cell design features a simple, symmetric layout that significantly reduces die size to lower costs. The MirrorBit architecture also uses a dramatically simpler manufacturing process, further reducing costs. Finally, the MirrorBit architecture scales easily with lithography, providing customers a clear
roadmap to future cost reductions. When it comes to cost, MirrorBit Flash outperforms both standard Flash and multi-level cell (MLC) technology.

**MirrorBit™ vs. MLC**

**How to Enhance the Storage Capacity of a Flash Device**

There are two ways to enhance the storage capacity of a Flash device:

1. Store full, distinct charge areas within each memory cell using MirrorBit technology.
2. Store fractional levels of charge in each memory cell using multi-level cell (MLC) technology.

Both result in high-density, low-cost Flash solutions, but only MirrorBit Flash doubles device density without compromising performance and data integrity.

**Performance Issues**

- **MirrorBit™**
  
  With the MirrorBit cell, the left bit and right bit are independently stored, independently programmed, and independently assessed—offering full-horsepower, full-margin programming and read capabilities. In fact, MirrorBit Flash delivers the same high read and write performance as our proven conventional Flash.

- **MLC**
  
  Multi-level cells store four charge levels—with the number of electrons determining units of data. Each charge level corresponds to a certain threshold voltage. When voltage greater than the threshold voltage is applied to the cell, current flows across the transistor.

  To program a multi-level cell, electrons need to be precisely metered into the floating gate. This creates a slow write process. Since the multi-level cell must distinguish between multiple threshold voltages, its read operation is also slow. Furthermore, pre-programming of the cells is required prior to erasure; and because MLC programming is intrinsically slow, erase operations are slow as well.

**Reliability Issues**

- **MirrorBit™**
  
  The MirrorBit architecture guarantees data retention.

  With the MirrorBit cell, electrons can be stored on either side of the cell—where they remain trapped. So, read, program, and erase operations are performed at full speed and power regardless of which side is being used.

  And, because each bit has a full operating margin, the MirrorBit cell behaves as two independent memory cells, with threshold voltage margins the same as that of single-bit Flash.

  As a result, MirrorBit Flash is inherently more reliable than MLC—because MirrorBit’s full voltage margin enables the same high levels of data retention as conventional NOR.

- **MLC**
  
  Since MLC technology depends on the number of electrons in the floating gate, a loss of electrons can cause data corruption and device failure.

  To ensure the basic cell has a sufficiently wide threshold voltage window, MLC devices require higher operating voltages. However, high electric fields cause oxide breakdown and other stresses that consequently limit the endurance of the device.

  In addition, MLC Flash devices require very narrow threshold voltage margins to accommodate four charge states. Over time, margin-drift blurs the difference between charge states, which can result in data loss.
The bottom line is MLC Flash devices can easily corrupt code or data critical to the operation of your system or application. In fact, MLC Flash manufacturers do not guarantee data retention.

**Conclusions**
The MirrorBit architecture delivers the low-cost structure of a multi-level cell solution without any of the drawbacks of MLC. In other words, MirrorBit Flash delivers:

- High endurance
- High levels of reliability
- Guaranteed data retention
- Fast random access
- Short programming times
- Short erase times

**Device Operation**

**How Does Flash Memory Work?**
Conventional Flash memory devices store data by holding charge in a floating gate. This so-called floating gate lies between the control gate and the silicon substrate and is surrounded by silicon dioxide. In a neutral state, there is no conductive path between the source and drain regions. But, when a positive voltage is applied to both the gate and drain, a channel begins to form in the cell. When the gate voltage is sufficiently large, the channel is completely formed and electrons flow from the source to the drain. The key to Flash memory cell operation is that when a charge is stored in the floating gate, the threshold voltage of the transistor increases. This change in threshold voltage allows you to detect whether data is stored in the memory cell.

**MirrorBit Architecture**
The MirrorBit cell stores two distinct and full units of charge within a single cell.

How?

The innovative MirrorBit cell architecture features a non-conducting storage element and identical, selectable source-drains.

With two distinct transistors in one cell, electrons can be independently stored in and read from either side of the cell.

**Write Operations**

- **Conventional Flash**
  To write to a conventional Flash cell, a large positive voltage is applied to the gate and drain, which sends electrons into the floating gate near the drain. Since the gate is conductive, electrons are distributed throughout the floating gate... so only one charge state can be stored in a single cell.

- **MirrorBit Flash**
  As with conventional Flash, writing information in a MirrorBit cell works by injecting electrons into the floating gate near the drain; however, since the storage element is non-conductive, the electrons are trapped on one side of the non-conductive storage element. The process can then be reversed for writing to the other side. Because of the symmetrical cell layout and selectable source-drains, distinct charge can be stored independently on either side.

**Read Operations**

- **Conventional Flash**
  A conventional Flash cell is read by applying a read reference voltage to the gate and drain. This voltage is higher than the threshold voltage of an unprogrammed cell but lower than the
threshold voltage of a programmed cell. So, a conductive channel forms and current flows if the Flash cell is unprogrammed, but not if the Flash cell is programmed.

- **MirrorBit Flash**
  MirrorBit Flash offers independent full-horsepower read operations from each side of the storage element. MirrorBit technology reads from the source side of the cell. This means when the source bit is programmed, no current flows and it reads as charged – just like a standard, programmed Flash memory cell. But when the source bit is unprogrammed, current flows and the bit reads as uncharged – just like a standard, unprogrammed Flash memory cell. This is true even if the other bit is programmed. A drain-side bias causes a conductive “depletion region” to extend on the drain side, so the conductive channel is unaffected by the stored charge – a channel still forms and the source bit is read as uncharged.

  And because the source-drains are selectable – which means the source can be on either side of the cell – each side of the storage element can be independently read in the same way.

**Erase Operations**
MirrorBit technology uses AMD’s patented and proven negative gate erase technique. Specifically, the negative gate and common positive voltages used during erasure are like those used in conventional Flash devices.

Note the left and right bits of a MirrorBit cell are always in the same sector, so an entire MirrorBit cell is erased during a sector- or chip-erase operation. To protect against over- or under-erasure, all bits in a sector are pre-programmed. And, AMD’s proven Embedded Erase algorithm automatically verifies erase margins.

**Summary**
To summarize, the innovative MirrorBit cell architecture:

- Utilizes a simple, symmetric design that stores two bits of data in two distinct charge areas in a single memory cell.
- Delivers independent, full-horsepower read and write operations for each of two bits within a memory cell.
- Operates on the same proven principles as AMD’s single-bit cell Flash.

**Cost Structure**

**MirrorBit Technology’s Patented Design Results in the Industry’s Best Cost Structure**
MirrorBit technology breaks the traditional trade-off between cost and performance. In fact, MirrorBit technology combines the high reliability and performance of AMD’s proven single-bit products with the industry’s leading cost structure.

**Why Is Our Cost Structure the Best in the Industry?**
There are two primary cost drivers: die size and process.

**Die Size**
Die size describes the wafer area required for a single Flash device. As die size shrinks, a single wafer produces more Flash devices, thereby lowering costs.

Die size is a function of two variables: lithography and memory array layout. Lithography determines the size of an individual transistor while the memory array layout determines how many transistors can be packed together within a given area. MirrorBit’s simple, symmetric cell architecture results in a significant improvement in cell density for a given area.

In addition, the MirrorBit architecture’s ability to scale easily with lithography ensures future cost structure improvements as lithography shrinks.
Process
MirrorBit technology utilizes a highly efficient manufacturing process to help deliver Flash memory with the industry's best cost structure. It involves fewer layers and fewer process steps.

As the number of steps involved in manufacturing decreases, so do the time and cost required in producing the wafer.

Compared to NOR and MLC, MirrorBit Flash offers:

- Simple topography
- Fewer process layers
- Fewer process steps

Result
MirrorBit technology's supreme combination of double storage capacity, small die sizes, and efficient processing make it the Flash solution with the industry's leading cost structure. In fact, quarter-micron MirrorBit Flash delivers a comparable cost-structure to .18-micron MLC. What's more, AMD's aggressive roadmap to .13-micron lithography will result in additional benefits in the near future.

Remarkably, MirrorBit Flash delivers the industry's LEADING COST STRUCTURE while maintaining the HIGH PERFORMANCE and RELIABILITY of AMD's single-bit products.

Migration to MirrorBit™

What's Available?
With densities between 16 megabits and 1 gigabit, MirrorBit technology provides an unparalleled migration path to high-density, low-cost Flash. In fact, consistent pin-outs and packages enable designers to migrate from 16 megabits to 1 gigabit MirrorBit Flash without having to change their boards. At the same time, multiple options for packaging and sector architecture - at each density - make MirrorBit Flash an ideal choice for a wide range of systems and applications. More importantly, most MirrorBit devices are fully compatible with AMD's single-bit per cell Am29LV devices, offering seamless integration, for immediate use with both new and existing designs.

How to Get Started
You can get started with MirrorBit Flash today. Simply contact your local AMD sales representative or click on one of the links to learn more.